MODULE DESCRIPTION FORM

Module Information					
Module Title	Advance Computer Architecture			**Module Delivery**	
Module Type	**Core**			☒ **Lecture** ☒ **Theory**	
Module Code	**IT3204**				
ECTS Credits	**4**				
SWL (hr/sem)	**100**				
Module Level	UGIII		**Semester of Delivery**	2	
Administering Department	Information Technology		**College**	College of Science	
Module Leader	Mahmood Jasim Khalsan Hadi		**e-mail**	mahmood.jasim@uowa.edu.iq	
Module Leader's Acad. Title	Lecturer		**Module Leader's Qualification**	Ph. D	
Module Tutor	Mahmood Jasim Khalsan Hadi		**e-mail**	mahmood.jasim@uowa.edu.iq	
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Scientific Committee Approval Date	2026/2025		**Version Number**	V1	

Relation with other Modules			
Prerequisite module	-	**Semester**	-
Co-requisites module	Non	**Semester**	-

جامعة وارث الانبياء
كلية العلوم
قسم تكنولوجيا المعلومات

2026 / 2025

جامعة وارث الانبياء
عمادة كلية العلوم

Department Head Approval **Dean of the College Approval**

Module Aims, Learning Outcomes and Indicative Contents

Module Objectives	The purpose of the course is to introduce the advanced concepts of computer architecture. Knowing the student, the basics of building a computer, building microprocessors, interconnecting and organizing the basic units that make up a computer system, and how the internal devices interact with each other and with input and output devices. Evaluate different memory handling mechanism, memory hierarchy design, storage systems. Review the state of the art of computer architecture and microprocessors. Comprehend the impact of different instruction set architectures on design decisions.
Module Learning Outcomes	1. During the course, the student learns the basics of building a computer. 2. Understand the basics of microprocessor development. 3. Learn how to choose the appropriate architecture to build the microprocessor and the basic parts of the computer. 4. The student learns how to deal with input and output devices as one of the basic parts of a computer system.
Indicative Contents	The course includes the following topics: **1. Advanced Description of Basic Microprocessor Architecture** Students study the detailed architecture of the microprocessor, including: • The main components and functional units of the processor. • Developments in computer architecture. • Moore's Law and its impact on processor evolution. • The fundamental levels upon which computer architecture is built. **2. Introduction to Modern Microprocessor Architectures** Students learn: • The basic computer design and its core functional units. • The Von Neumann and Harvard architectures as foundational models. • Data movement between processor and memory. • Processor performance concepts and methods of performance evaluation. **3. Concept of the Machine Cycle** Students study: • The detailed stages of the machine cycle. • Data transfer between memory and registers. • Different cycle types within the computer system. • Methods for calculating processor efficiency based on Iron's Law. • Key factors affecting processor performance. **4. CPU Performance Calculation** Students learn: • Methods for calculating processor efficiency based on instruction count and clock cycles. • The relationship between executed instructions and total execution time. • Processor speed calculation using Amdahl's Law. **5. MIPS Architecture**

	Students explore: • The architectural structure of MIPS. • Instruction formats and types. • Instruction execution within the computer system. • Instruction set design and organization.
	6. MIPS Assembly Language Students learn: • Assembly language and machine language concepts. • Translation between high-level and low-level languages. • Memory addressing techniques. • Jump and branch instructions.
	7. MIPS Microarchitecture Students study: • Internal components of the MIPS system. • The Datapath structure. • Control signals and their role in managing instruction execution.
	8. CISC, RISC, and Superscalar Architectures Students understand: • Differences between Complex Instruction Set Computing (CISC) and Reduced Instruction Set Computing (RISC). • Superscalar processor concepts. • Data access methods in memory. • Instruction complexity and programming implications.
	9. Flynn's Classification Students learn: • Advanced processing techniques. • Parallel processing systems. • Flynn's taxonomy (SISD, SIMD, MISD, MIMD) and system classification.

Learning and Teaching Strategies	
Strategies	The learning and teaching strategies for studying the advanced computer architecture in an IT department involve scientific discussions and dialogues and asking questions between the students. Demonstrate how to deal with the basic parts of a computer system, how the processor interacts with the rest of the computer. Familiarity with the basic concepts of the mechanism of data transmission, processing and storage in the system. Knowledge with the way the central control unit and the recorders work inside the processor chip These strategies ensure a comprehensive understanding of internal architecture of microprocessor and their relevance in the IT field.

Student Workload (SWL)			
Structured SWL (h/sem)	45	**Structured SWL (h/w)**	3
Unstructured SWL (h/sem)	52	**Unstructured SWL (h/w)**	3.5
Total SWL (h/sem)	97 + **3 final** = 100		

Module Evaluation					
		Time/Number	**Weight (Marks)**	**Week Due**	**Relevant Learning Outcome**
Formative assessment	**Quizzes**	5	15% (10)	2,3,8,10,14	Students will be able to recall and explain fundamental concepts and key terminology of the course.
	Homework assignment	2	10% (10)	5,12	Students will be able to apply theoretical knowledge to solve structured practical problems independently.
	Report	1	5% (10)	13	Students will be able to analyze and synthesize information to produce a well-structured academic report supported by credible sources.
	Seminar	1	10% (10)	Continuous	Students will be able to present and defend academic ideas clearly and professionally in front of an audience.
Summative assessment	**Midterm Exam**	2hr	10% (10)	7	All
	Final Exam	3hr	50% (50)	16	All
Total assessment			100% (100 Marks)		

Delivery Plan (Weekly Syllabus)	
	Material Covered
Week 1	**Fundamentals of Computer Design** • Classes of Computers • Evolution of Computers • Moore's Law • Abstraction Layers in Modern Systems
Week 2	**Basic Computer Design** • Von Neumann Architecture • Harvard Architecture
Week 3	**Machine Cycle & Early Architectures** • The Fetch–Execute Cycle • Architecture of the IAS Computer • How the CPU Performs the Machine Cycle • CPU Performance Definition
Week 4	**CPU Performance Metrics** • Instruction Types and CPI • Instruction Frequency and CPI • Amdahl's Law
Week 5	**Instruction Set Architecture (ISA)** • Introduction to ISA • MIPS Architecture Overview • Introduction to MIPS Instructions
Week 6	**MIPS Instruction Structure** • MIPS Instruction Format • MIPS Instruction Groups
Week 7	**MIPS Programming Fundamentals** • MIPS Machine Language • MIPS Assembly Language • Translating High-Level Code to MIPS Assembly • Translating MIPS Assembly to Machine Code • Address Calculation in Branch and Jump Instructions
Week 8	**Instruction Execution Process** • Phases of Instruction Execution

Week 9	**Advanced CPU Performance Analysis** • Iron Law of Processor Performance • Three Components for Measuring CPU Performance
Week 10	**MIPS Microarchitecture** • Computer Configuration for MIPS • MIPS Instruction Cycle Implementation • Datapath Design and Implementation • Control Unit for MIPS • ALU Operations and Internal Data Transfer
Week 11	**MIPS Addressing Modes**
Week 12	**Processor Architectures** • CISC Architecture • RISC Architecture
Week 13	**Processing Techniques** • Serial Processing • Introduction to Parallel Processing
Week 14	**Parallel Processing Classification** • Flynn's Classification (SISD, SIMD, MISD, MIMD)
Week 15	**MIPS Pipeline Design** • Introduction to Pipelining • Designing MIPS for Pipelining
Week 16	**Preparatory Week** • Review and Preparation for Final Exam

Learning and Teaching Resources		
	Text	**Available in the Library?**
Required Texts	• J.L. Hennessy and D.A. Patterson. Computer Architecture: A Quantitative Approach, 6th Edition, Morgan Kaufmann, 2019	Yes
Recommended Texts	• Advanced computer architecture and parallel processing (Hesham El-Rewini, Mostafa Abd-ElBarr) ,2015 • Advanced Computer Architecture Kai Hwang 2nd edition 2008	Yes

	• Computer Organization and Design 4th by J.L. Hennessy and D.A. Patterson.2009 • Fundamentals of Computer Design	
Websites		

Grading Scheme				
Group	**Grade**	**Appreciation**	**Marks %**	**Definition**
Success Group (50 - 100)	**A -** Excellent	Excellent	90 - 100	Outstanding Performance
	B - Very Good	Very Good	80 - 89	Above average with some errors
	C - Good	Good	70 - 79	Sound work with notable errors
	D - Satisfactory	Fair / Average	60 - 69	Fair but with major shortcomings
	E - Sufficient	Pass / Acceptable	50 - 59	Work meets minimum criteria
Fail Group (0 – 49)	**FX** – Fail	Fail (Pending)	(45-49)	More work required but credit awarded
	F – Fail	Fail	(0-44)	Considerable amount of work required

Note: Marks Decimal places above or below 0.5 will be rounded to the higher or lower full mark (for example a mark of 54.5 will be rounded to 55, whereas a mark of 54.4 will be rounded to 54. The University has a policy NOT to condone "near-pass fails" so the only adjustment to marks awarded by the original marker(s) will be the automatic rounding outlined above.